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Patent
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Keeth, et al.	**Examiner:**	Tran, M.
Serial No.:	09/899,977	**Art Unit:**	2818
Filed:	6 July 2001		

Entitled: 256 MEG DYNAMIC RANDOM ACCESS MEMORY

THIRD PRELIMINARY AMENDMENT

Preliminary to the examination of the above-identified application, please amend the claims as follows.

167[166]. (Once Amended) The memory of claim 70 wherein said array is organized into rows and columns to form a plurality of individual arrays, and wherein said plurality of individual arrays is organized into a plurality of array blocks, and wherein said plurality of peripheral devices includes a plurality of sense amplifiers positioned between adjacent rows of individual arrays and a plurality of row decoders positioned between adjacent columns of individual arrays.

168[167]. (Once Amended) The memory of claim 167[166] wherein each of said plurality of individual arrays includes digitlines extending therethrough and into said sense amplifiers, and wherein said array blocks include I/O lines running between adjacent rows of individual arrays and through said sense amplifiers, said sense amplifiers including circuits for transferring signals on said digitlines to said I/O lines.

169[168]. (Once Amended) The memory of claim 70 wherein said array of memory cells is organized into a plurality of array blocks, said memory additionally comprising a power distribution bus including a first plurality of conductors forming a web around each of said array blocks and a second plurality of conductors extending from said web to form a grid within each of said array blocks.